IN THE CLAIMS

A marked up version of the claims as amended is set forth below.

Please amend the claims as follows:

1. (Currently amended) A method for fabricating a bipolar transistor comprising:

forming an emitter region in a first epitaxial layer;

etching the first epitaxial layer using an emitter pedestal structure which includes sidewall spacers as a masking member so as to undercut the emitter pedestal structure; and

growing a second epitaxial layer on the first epitaxial layer.

2. **(Cancelled)**

3. (Currently amended) The method defined by claim [[2]] 1, wherein a second epitaxial layer is more heavily doped than the first epitaxial layer.

4. (Currently amended) The method defined by claim 1, including:

forming a polysilicon layer on an oxide layer having an opening which exposes the emitter region;

defining an emitter pedestal from the polysilicon layer; and

forming oxide sidewall spacers on the emitter pedestal, thereby forming the pedestal structure.

5. (Original) The method defined by claim 4, wherein the first epitaxial layer is a silicon-germanium layer.

6. (Original) The method defined by claim 5, wherein the second epitaxial layer is a silicon-germanium layer.

7. (Original) A method for fabricating a bipolar transistor comprising:

forming a first epitaxial layer over a collector region;

forming an emitter region in the first epitaxial layer and an emitter pedestal above the first epitaxial layer;

forming sidewall spacers on the emitter pedestal over the first epitaxial layer;

etching the first epitaxial layer including undercutting the sidewall spacers; and

growing a second epitaxial layer on the first epitaxial layer.

8. (Original) The method defined by claim 7, wherein the first and second epitaxial layers are doped with a first conductivity type dopant.

9. (Original) The method defined by claim 8, wherein the second epitaxial layer is doped more heavily than the first epitaxial layer with the first conductivity type dopant.

10. (Original) The method defined by claim 9, wherein the second epitaxial layer is grown to a level above an upper level of the first epitaxial layer.

11. (Original) The method defined by claim 9, wherein the first and second epitaxial layers comprise silicon-germanium.

12. (Original) The method defined by claim 7, wherein the emitter pedestal is formed from a polysilicon layer doped with a second conductivity type dopant.

13. (Original) The method defined by claim 12, wherein the formation of the emitter region and emitter pedestal includes:

forming an oxide layer on the first epitaxial layer;

defining an opening in the oxide layer for the emitter region;

forming the polysilicon layer over the oxide layer; and

driving the second conductivity type dopant from the polysilicon layer into the first epitaxial layer to define the emitter region.

14. (Original) The method defined by claim 7, wherein the etching comprises use of an isotropic etchant.

15. (Original) The method of claim 7, wherein the first epitaxial layer includes the intrinsic base region and at least part of the link based region for the transistor.

16. (Original) The method defined by claim 15, wherein the second epitaxial layer comprises the extrinsic base region for the transistor.

Claims 17-22 (Cancelled)